

## CLAIMS

- 1 1. An integrated circuit comprising:  
2 an I/O pad of a first type made of a deposited conductor, wherein the I/O pad of the  
3 fist type is connected to a first point on the integrated circuit;  
4 a strip of deposited conductor closely adjacent to the I/O pad of the fist type, wherein  
5 the strip of conductor is connected to a second point on the integrated circuit
- 1 2. The integrated circuit of claim 1, wherein the I/O pad of the first type is selected from a  
2 group consisting of a data I/O pad, a multi-level I/O pad and a power supply I/O pad.
- 1 3. The integrated circuit of claim 1, wherein the first point on the integrated circuit is further  
2 connected to a circuitry.
- 1 4. The integrated circuit of claim 1, wherein the first point on the integrated circuit is further  
2 connected to a power bus.
- 1 5. The integrated circuit of claim 1, wherein the second point on the integrated circuit is  
2 further connected to a circuitry.
- 1 6. The integrated circuit of claim 1, wherein the second point on the integrated circuit is  
2 further connected to a power bus.
- 1 7. The integrated circuit of claim 1, wherein the strip of conductor is connected to a third  
2 point on the integrated circuit.
- 1 8. The integrated circuit of claim 7, wherein the second and third points on the integrated  
2 circuit are connected to a circuitry.
- 1 9. The integrated circuit of claim 7, wherein the second and third points on the integrated  
2 circuit are connected to a power bus.

1 10. The integrated circuit of claim 1, further comprising an I/O pad of a second type made of  
2 a deposited conductor, wherein the I/O pad of the second type is connected to third point on  
3 the integrated circuit.

1 11. The integrated circuit of claim 10, wherein the I/O pad of the second type is selected  
2 from a group consisting of a data I/O pad, a multi-level I/O pad and a power supply I/O pad.

1 12. The integrated circuit of claim 10, wherein the third point on the integrated circuit is  
2 further connected to a circuitry.

1 13. The integrated circuit of claim 10, wherein the third point on the integrated circuit is  
2 further connected to a power bus.

1 14. The integrated circuit of claim 10, wherein the strip of conductor is connected to a fourth  
2 point on the integrated circuit.

1 15. The integrated circuit of claim 14, wherein the second, third and fourth points on the  
2 integrated circuit are connected to a circuitry.

1 16. The integrated circuit of claim 14, wherein the second, third and fourth points on the  
2 integrated circuit are connected to a power bus.

1 17. The integrated circuit of claim 1, wherein the I/O pad of the first type provides power to  
2 a core circuitry.

1 18. The integrated circuit of claims 4, 6, 9, 13 or 16, wherein the power bus is configured as  
2 an intersecting grid of a deposited conductor.

1 19. The integrated circuit of claim 18, wherein the integrated circuit is comprised of multiple  
2 metal layers, and wherein the I/O pad of the first type and the power bus are deposited on  
3 different layers.

1 20. The integrated circuit of claim 19, wherein the power bus exists at a lowest layer.

1 21. The integrated circuit of claim 19, wherein the power bus exists at a second to lowest  
2 layer.

1 22. An integrated circuit comprising:  
2 a power supply I/O pad made of a deposited conductor;  
3 a power bus connected to the power supply I/O pad;  
4 a data I/O pad made of a deposited conductor;  
5 circuitry connected to the data I/O pad; and  
6 a strip of deposited conductor closely adjacent to the data I/O pad wherein the strip of  
7 conductor is connected to multiple points on the power bus.

1 23. The integrated circuit of claim 22, wherein the power bus provides power to a core  
2 circuitry.

1 24. The integrated circuit of claim 22, wherein the power bus is configured as an intersecting  
2 grid of a deposited conductor.

1 25. The integrated circuit of claim 22, wherein the integrated circuit is comprised of multiple  
2 metal layers, and wherein the power supply I/O pad and the power bus are deposited on  
3 different layers.

1 26. The integrated circuit of claim 25, wherein the power buss exists at the lowest layer.

1 27. The integrated circuit of claim 25, wherein the power bus exists at the second to the  
2 lowest layer.

1 28. An integrated circuit comprising:  
2 a power supply I/O pad made of a deposited conductor;  
3 a power bus connected to the power supply I/O pad;  
4 a multi-level voltage I/O pad made of a deposited conductor;  
5 circuitry connected to the multi-level voltage I/O pad; and  
6 a strip of deposited conductor closely adjacent to the multi-level I/O pad wherein the  
7 strip of conductor is connected to multiple points on the power bus.

1 29. The integrated circuit of claim 28, wherein the power bus provides power to a core  
2 circuitry.

1 30. The integrated circuit of claim 28, wherein the power bus is configured as an intersecting  
2 grid of a deposited conductor.

1 31. The integrated circuit of claim 28, wherein the integrated circuit is comprised of multiple  
2 metal layers, and wherein the power supply I/O pad and the power bus are deposited on  
3 different layers.

1 32. The integrated circuit of claim 31, wherein the power buss exists at the lowest layer.

1 33. The integrated circuit of claim 31, wherein the power bus exists at the second to the  
2 lowest layer.

1 34. An integrated circuit comprising:

2 a positive power supply I/O pad made of a deposited conductor;  
3 a positive power bus connected to the positive power supply I/O pad;  
4 a negative power supply I/O pad made of a deposited conductor;  
5 a negative power bus connected to the negative power supply I/O pad;  
6 a data or multi-level voltage I/O pad made of a deposited conductor;  
7 circuitry connected to the data or multi-level voltage I/O pad;  
8 a first strip of deposited conductor closely adjacent to the data or multi-level I/O pad  
9 wherein the strip of conductor is connected to multiple points on the positive power bus; and  
10 a second strip of deposited conductor closely adjacent to the data or multi-level I/O  
11 pad wherein the strip of conductor is connected to multiple points on the negative power bus.

1 35. The integrated circuit of claim 34, wherein the power buses provide positive and  
2 negative power to a core circuitry.

1 36. The integrated circuit of claim 34, wherein the power buses are configured as  
2 intersecting grids of a deposited conductor.

1 37. The integrated circuit of claim 34, wherein the integrated circuit is comprised of multiple  
2 metal layers, and wherein the positive and negative power buses are deposited on third and  
3 fourth layers, respectively.

1 38. The integrated circuit of claim 34, wherein the integrated circuit is comprised of multiple  
2 metal layers, and wherein the positive and negative power supply I/O pads are deposited on a  
3 first and second layer, respectively.

1 39. The integrated circuit of claim 38, wherein the first and second layers are the same layer.

1 40. The integrated circuit of claim 38, wherein the negative power bus exists at the lowest  
2 layer.

1 41. The integrated circuit of claim 38, wherein the positive power bus exists at the lowest  
2 layer.

1 42. The integrated circuit of claim 38, wherein the negative power bus exists at the second  
2 lowest layer.

1 43. The integrated circuit of claim 38, wherein the negative and positive power buses are  
2 further deposited on a fifth and sixth layer.

1 44. The integrated circuit of claim 38, wherein the positive power bus exists at the second  
2 lowest layer.

1 45. The integrated circuit of claim 44, wherein the negative power bus exists at the third  
2 lowest layer.

1 46. The integrated circuit of claim 44, wherein the positive power bus exists at the third  
2 lowest layer.

1 47. The integrated circuit of claim 44, wherein the negative power bus exists at the fourth  
2 lowest layer.

